

# ABSTRACT OF THE DISCLOSURE

Circuitry is provided for controlling the slew rate of a negative output supply. The slew rate control circuitry includes an NMOS FET, a feedback resistor connected across the drain and the gate of the NMOS FET, an input resistor connected to the gate of the NMOS FET, level shifting circuitry connected between a positive output supply voltage and the input resistor, and a bias current source connected to the gate of the NMOS FET. A negative input supply voltage is connected to the source of the NMOS FET, and the negative output supply voltage is provided across a load connected to the drain of the NMOS FET. As the positive supply voltage ramps up from 0 to  $+V_s$ , the level shifter provides a voltage to the input resistor that ramps up from  $-V_s$  to 0 volts. Further, the drain voltage of the NMOS FET ramps down from 0 to  $-V_s$ , thereby providing a negative output supply voltage  $-V_s$  with a slew rate that linearly tracks the slew rate of the master positive output supply.

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